X0022

N-Channel Enhancement Mode MOSFET

40V(VDS) / ±20V(VGS) /6A(ID)

Rev0.9

Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0022	**40V(V_{DS}) / ±20V(V_{GS}) / 6A(I_D)** **N-Channel Enhancement Mode MOSFET**	36,000

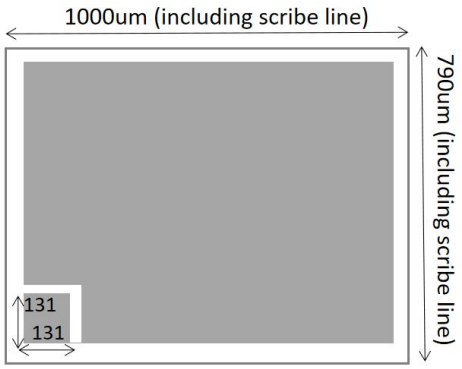
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kA°)
Nominal Front Metal Composition, Thickness	AlCu (4μm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	150±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at Tj = 25 °C, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			V	V_{GS}=0V, I_D=250μA
I_D (Device Ref)	Continuous Drain Current			6	A	T_J=25℃
$R_{DS(on)}$(CP)	Static Drain-to-Source On-Resistance		21	27	mΩ	V_{GS}=10V, I_D=1A
			25	36	mΩ	V_{GS}=4.5V, I_D=1A
$R_{DS(on)}$(FT)	Static Drain-to-Source On-Resistance		23	30	mΩ	V_{GS}=10V, I_D=4A
			27	40	mΩ	V_{GS}=4.5V, I_D=3A
$V_{GS(th)}$	Gate Threshold Voltage	1	1.4	1.7	V	V_{DS}=V_{GS}, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current			1	μA	V_{DS}=40V, V_{GS}=0V
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	V_{GS}=±20V, V_{DS}=0V
T_J, T_{STG}	Operating and Storage Temperature	-55℃ to 150℃ Max				

4. Die Outline



Die Size: 1000μm × 790μm (including scribe line)

Gate: 131μm × 131μm

For SOP8 package

Suggest Bonding wire:

Gate: 1 × 1.0 mil Cu

Source: 12× 1.65 mil Cu