

X0034

N-Channel Enhancement Mode MOSFET

40V(VDS) / ± 20 V(VGS) / 9A(ID)

Rev1.4



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0034	40V(V_{DS}) / $\pm 20V(V_{GS})$ / 9A(I_D) N-Channel Enhancement Mode MOSFET	29,856

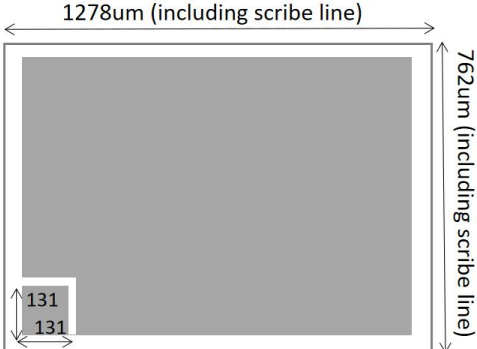
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kÅ°)
Nominal Front Metal Composition, Thickness	AlCu (4µm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	150±10µm
Scribe Line Width	60µm
Passivation	SiN+SiO ₂

3. Key Electrical Characteristics of Die (at T_J = 25 °C, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			V	$V_{GS}=0V$, $I_D=250\mu A$
I_D (Device Ref)	Continuous Drain Current			9	A	$T_J=25^\circ C$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		18	24	mΩ	$V_{GS}=10V$, $I_D=1A$
			24	35	mΩ	$V_{GS}=4.5V$, $I_D=1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		19	25	mΩ	$V_{GS}=10V$, $I_D=5A$
			25	36	mΩ	$V_{GS}=4.5V$, $I_D=3A$
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.7	2.5	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1	µA	$V_{DS}=40V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 1278µm × 762µm (including scribe line)
	Gate: 131µm × 131µm
	For SOP8 package Suggest Bonding wire: Gate: 1 × 1.0 mil Cu Source: 12 × 1.65 mil Cu