

X0050

N-Channel Enhancement Mode MOSFET

40V(VDS) / ± 20 V(VGS) / 5A(ID)

Rev0.6



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0050	40V(V_{DS}) / $\pm 20V(V_{GS})$ / 5A(I_D) N-Channel Enhancement Mode MOSFET	43,878

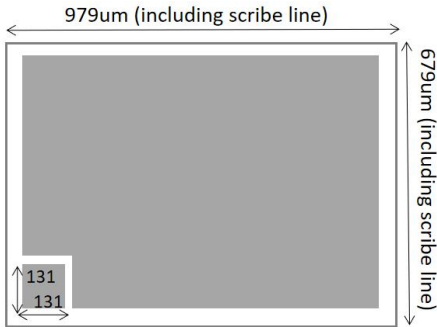
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kÅ°)
Nominal Front Metal Composition, Thickness	AlCu (4μm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	150±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			V	$V_{GS}=0V$, $I_D=250\mu A$
I_D (Device Ref)	Continuous Drain Current			5	A	$T_J=25^\circ\text{C}$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		27	37	mΩ	$V_{GS}=10V$, $I_D=1A$
			35	47	mΩ	$V_{GS}=4.5V$, $I_D=1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		30	40	mΩ	$V_{GS}=10V$, $I_D=5A$
			38	50	mΩ	$V_{GS}=4.5V$, $I_D=3A$
$V_{GS(th)}$	Gate Threshold Voltage	1.3	1.9	2.3	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1	μA	$V_{DS}=40V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 979μm × 679μm (including scribe line)
	Gate: 131μm × 131μm
	For SOT-23 package Suggest Bonding wire: Gate: 1 × 1.0 mil Cu Source: 6 × 1.65 mil Cu