X0068

N-Channel Enhancement Mode MOSFET

20V(VDS) / ±12V(VGS) / 4A(ID)

Rev1.0

Wafer Specification

1.Order Information

Part No.	Description	Gross die/per 8"wafer
X0068	**20V(V_{DS})/±12V(V_{GS})/4A(I_D)** **N-Channel Enhancement Mode MOSFET**	125,000

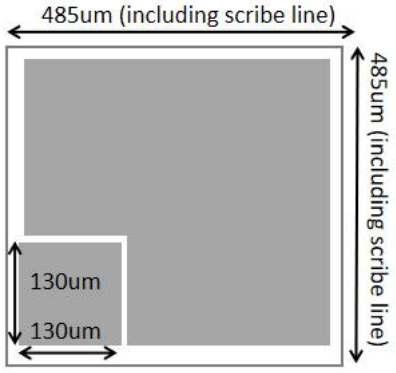
2.Mechanical Data

Nominal Back Metal Composition,Thickness	Ti-Ni-Ag(13kA°)
Nominal Front Metal Composition,Thickness	AlCu(4μm)
Wafer Diameter	200mm,with 010 notch
Wafer Thickness	150±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3.Key Electrical Characteristics of Die(at Tj=25°C,unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20			V	V_{GS}=0V,I_D=250μA
I_D(Device Ref)	Continuous Drain Current			4	A	T_J=25℃
$R_{DS(on)}$(CP)	Static Drain-to-Source On-Resistance		30	40	mΩ	V_{GS}=4.5V,I_D=1A
			37	55	mΩ	V_{GS}=2.5V,I_D=1A
$R_{DS(on)}$(FT)	Static Drain-to-Source On-Resistance		36	44	mΩ	V_{GS}=4.5V,I_D=3A
			43	59	mΩ	V_{GS}=2.5V,I_D=1A
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.7	1.0	V	V_{DS}=V_{GS},I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current			1	μA	V_{DS}=20V,V_{GS}=0V
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	V_{GS}=±12V,V_{DS}=0V
T_J,T_{STG}	Operating and Storage Temperature	-55℃to 150℃Max				

4.Die Outline



Die Size:485μm×485μm(including scribe line)

Gate:130μm×130μm

For SOT-23 package

Suggest Bonding wire:

Gate: 1×1.0 mil Cu

Source: 4×1.65 mil Cu