

X0107

N-Channel Enhancement Mode MOSFET

40V(VDS) / ± 20 V(VGS) / 210A(ID)

Rev0.1



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0108	40V(V_{DS}) / $\pm 20V(V_{GS})$ / 210A(I_D) N-Channel Enhancement Mode MOSFET	2,200

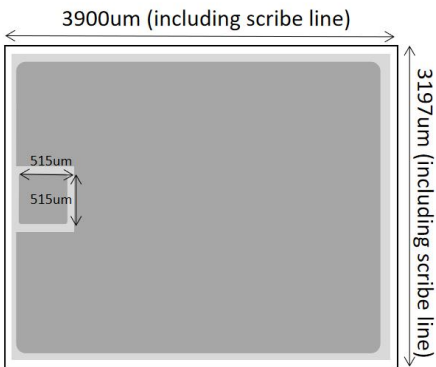
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kÅ°)
Nominal Front Metal Composition, Thickness	AlCu (4µm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	125±10µm
Scribe Line Width	60µm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			V	$V_{GS}=0V$, $I_D=250\mu A$
I_D (Device Ref)	Continuous Drain Current			210	A	$T_J=25^\circ\text{C}$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		1.8	8	mΩ	$V_{GS}=10V$, $I_D=1A$
			2.0	10	mΩ	$V_{GS}=8V$, $I_D=1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		1.9	2.5	mΩ	$V_{GS}=10V$, $I_D=30A$
			2.1	2.7	mΩ	$V_{GS}=8V$, $I_D=20A$
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.8	4.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1	µA	$V_{DS}=40V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 3900µm × 3197µm (including scribe line)
	Gate: 515µm × 515µm
	For PDFN5X6-8L AL Ribbon package Suggest Bonding wire: Gate: Cu 2mil*1 Source: AL 80*6mil*1