

X0125

N-Channel Enhancement Mode MOSFET

60V(VDS) / ± 20 V(VGS) / 90A(ID)

Rev0.2



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0125	60V(V_{DS}) / $\pm 20V(V_{GS})$ / 90A(I_D) N-Channel Enhancement Mode MOSFET	3,501

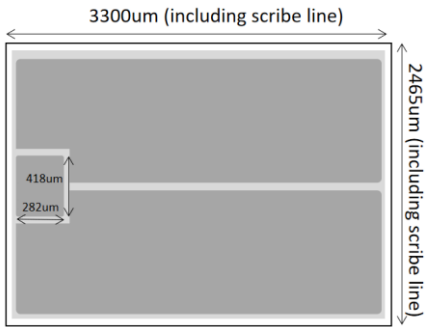
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kÅ°)
Nominal Front Metal Composition, Thickness	AlCu (4µm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	150µm
Scribe Line Width	60µm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60			V	$V_{GS}=0V$, $I_D=250\mu A$
I_D (Device Ref)	Continuous Drain Current			90	A	$T_J=25^\circ\text{C}$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		3.4	12	mΩ	$V_{GS}=10V$, $I_D=1A$
			4.1	15	mΩ	$V_{GS}=8V$, $I_D=1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		3.5	4.4	mΩ	$V_{GS}=10V$, $I_D=30A$
			4.2	5.3	mΩ	$V_{GS}=8V$, $I_D=30A$
$V_{GS(th)}$	Gate Threshold Voltage	2	3	4	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1	µA	$V_{DS}=60V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 3300µm × 2465µm (including scribe line)
	Gate: 282µm × 418µm
	For PDFN5x6-8L AL Ribbon package Suggest Bonding wire: Gate: 1 × 1.7 mil Cu Source: 6mil × 80 mil AL 