X0126

N-Channel Enhancement Mode MOSFET

68(VDS) / ±20V(VGS) /90A(ID)

Rev0.1

Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0126	**68V(V_{DS}) / ±20V(V_{GS}) /90A(I_D)** **N-Channel Enhancement Mode MOSFET**	3,501

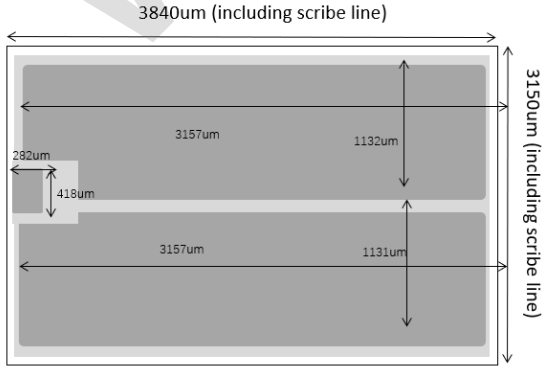
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (1kÅ-2kÅ-10kÅ
Nominal Front Metal Composition, Thickness	AlCu (4μm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	150±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at Tj = 25 °C, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	68			V	V_{GS}=0V, I_D=250μA
I_D (Device Ref)	Continuous Drain Current			30	A	T_J=25℃
$R_{DS(on)}$(CP)	Static Drain-to-Source On-Resistance		5.9	7.5	mΩ	V_{GS}=10V, I_D=1A
			6.2	7.9	mΩ	V_{GS}=8V, I_D=1A
$R_{DS(on)}$(FT)	Static Drain-to-Source On-Resistance		6.2	7.8	mΩ	V_{GS}=10V, I_D=30A
			6.5	8.2	mΩ	V_{GS}=8V, I_D=30A
$V_{GS(th)}$	Gate Threshold Voltage	2	3	4	V	V_{DS}=V_{GS}, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current			1	μA	V_{DS}=68V, V_{GS}=0V
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	V_{GS}=±20V, V_{DS}=0V
T_J, T_{STG}	Operating and Storage Temperature	-55℃ to 150℃ Max				

4. Die Outline



Die Size: 3300μm ×2465μm (including scribe line)

Gate: 282μm × 418μm

For PDFN5x6-8LAL Ribbon package

Suggest Bonding wire:

Gate: Cu 1*1.7mil*1

Source: AL 80mil*6mil*1