

X0132

N-Channel Enhancement Mode MOSFET

20V(VDS) / ± 12 V(VGS) / 2A(ID)

Rev0.1



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X0132	20V(V_{DS}) / $\pm 12V(V_{GS})$ / 2A(I_D) N-Channel Enhancement Mode MOSFET	200,000

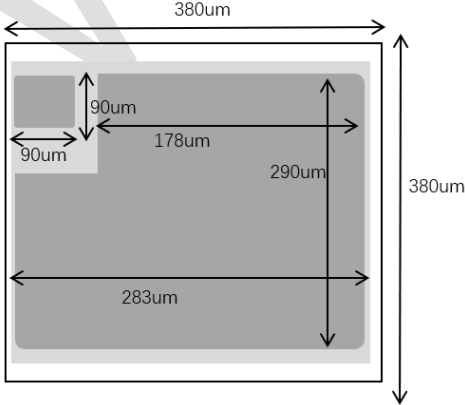
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (1kÅ-2kÅ-10kÅ)
Nominal Front Metal Composition, Thickness	AlCu (4μm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	125±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at Tj = 25 °C, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20			V	$V_{GS}=0V$, $I_D=250\mu A$
I_D (Device Ref)	Continuous Drain Current			30	A	$T_J=25^\circ C$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		45	54	mΩ	$V_{GS}=4.5V$, $I_D=1A$
			53	65	mΩ	$V_{GS}=2.5V$, $I_D=1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		48	58	mΩ	$V_{GS}=4.5V$, $I_D=1A$
			57	69	mΩ	$V_{GS}=2.5V$, $I_D=1A$
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.7	0.9	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1	μA	$V_{DS}=12V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 12V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 380μm × 380μm (including scribe line)
	Gate: 90μm × 90μm
	For DFN2020-6L package Suggest Bonding wire: Gate: 1*1.2mil Cu Source: 1*1.2mil Cu 