X1067

N-Channel Enhancement Mode MOSFET

19V(VDS) / ±10V(VGS) / 4A(ID)

Rev1.0

Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X1067	**19V(V_{DS}) / ±10V(V_{GS}) / 4A(I_D)** **N-Channel Enhancement Mode MOSFET**	54,826 (Dual)

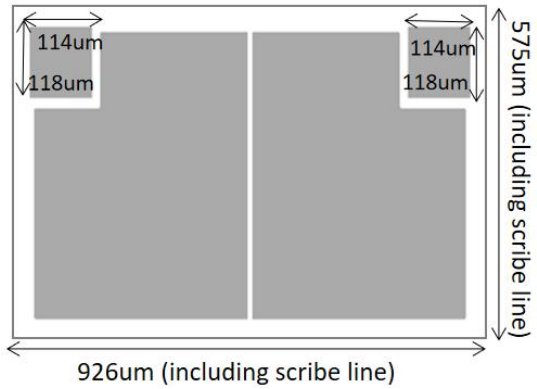
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kA°)
Nominal Front Metal Composition, Thickness	AlCu (4μm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	110μm±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die（at Tj = 25 °C, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	18	19		V	V_{GS}=0V, I_D=250μA
$I_{D(Device\ Ref)}$	Continuous Drain Current			4	A	T_J=25℃
$R_{DS(on)}$(CP)	Static Drain-to-Source On-Resistance		15	19,5	mΩ	V_{GS}=4.5V, I_D=1A
			21	28	mΩ	V_{GS}=2.5V, I_D=1A
$R_{DS(on)}$(FT)	Static Drain-to-Source On-Resistance		18	22.5	mΩ	V_{GS}=4.5V, I_D=3A
			24	31	mΩ	V_{GS}=2.5V, I_D=2A
$V_{GS(th)}$	Gate Threshold Voltage	0.45	0.75	1.05	V	V_{DS}=V_{GS}, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current			1	μA	V_{DS}=18V, V_{GS}=0V
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	V_{GS}=±10V, V_{DS}=0V
T_J, T_{STG}	Operating and Storage Temperature	-55℃ to 150℃ Max				

4. Die Outline



Die Size: 926μm × 575μm
(including scribe line)

Gate: 118μm × 114μm

For SOT23-6 package
Suggest Bonding wire:
Gate: 1 × 1.0 mil Cu *2
Source: 5 × 1.2 mil Cu *2