

X1096

N-Channel Enhancement Mode MOSFET

14V(VDS) / ± 10 V(VGS) / 2A(ID)

Rev0.7



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
X1096	14V(V_{DS}) / $\pm 10V(V_{GS})$ / 2A(I_D) N-Channel Enhancement Mode MOSFET	68,000 (Dual)

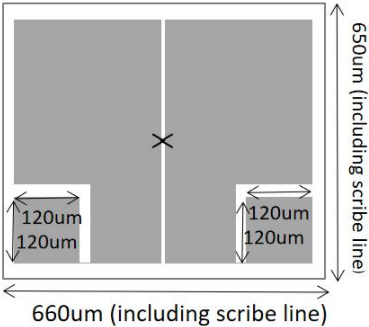
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag (13kÅ°)
Nominal Front Metal Composition, Thickness	AlCu (4µm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	125±10µm
Scribe Line Width	60µm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	14	16		V	$V_{GS}=0V$, $I_D=250\mu A$
I_D (Device Ref)	Continuous Drain Current			2	A	$T_J=25^\circ\text{C}$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		18	35	mΩ	$V_{GS}=4.5V$, $I_D=1A$
			25	45	mΩ	$V_{GS}=2.5V$, $I_D=1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		18	24	mΩ	$V_{GS}=4.5V$, $I_D=2A$
			22	30	mΩ	$V_{GS}=2.5V$, $I_D=1A$
$V_{GS(th)}$	Gate Threshold Voltage	0.4	0.7	1.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1	µA	$V_{DS}=12V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 10V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 650µm × 660µm (including scribe line)
	Gate: 120µm × 120µm
	For SOT23-6 package Suggest Bonding wire: Gate: 1 × 1.0 mil Cu *2 Source: 5 × 1.65 mil Cu *2