# X1097

# N-Channel Enhancement Mode MOSFET

**14V(VDS) / ±12V(VGS) / 2A(ID)**

**Rev0.5**



# Wafer Specification

## 1. Order Information

| Part No. | Description | Gross die / per 8" wafer |
|---|---|---|
| X1097 | **14V($V_{DS}$) / ±12V($V_{GS}$) / 2A($I_D$)**<br>**N-Channel Enhancement Mode MOSFET** | 74,000 (Dual) |

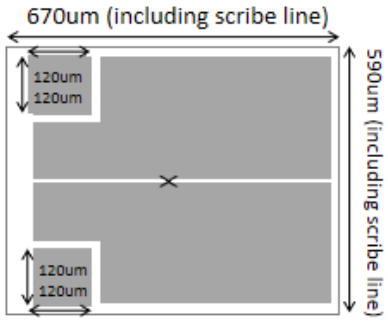
## 2. Mechanical Data

| | |
|---|---|
| Nominal Back Metal Composition, Thickness | Ti-Ni-Ag (1kA°-3kA°-8kA°) |
| Nominal Front Metal Composition, Thickness | AlCu (4μm) |
| Wafer Diameter | 200mm, with 010 notch |
| Wafer Thickness | 110±10μm |
| Scribe Line Width | 60μm |
| Passivation | SRO+SiN |

## 3. Key Electrical Characteristics of Die (at Tj = 25 °C, unless otherwise specified)

| Parameter | Description | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 14 | 17 | | V | $V_{GS}$=0V, $I_D$=250μA |
| $I_D$ (Device Ref) | Continuous Drain Current | | | 2 | A | $T_J$=25℃ |
| $R_{DS(on)}$(CP) | Static Drain-to-Source On-Resistance | | 15.5 | 20 | mΩ | $V_{GS}$=4.5V, $I_D$=1A |
| | | | 20 | 30 | mΩ | $V_{GS}$=2.5V, $I_D$=1A |
| $R_{DS(on)}$(FT) | Static Drain-to-Source On-Resistance | | 19.5 | 24 | mΩ | $V_{GS}$=4.5V, $I_D$=2A |
| | | | 24 | 34 | mΩ | $V_{GS}$=2.5V, $I_D$=1A |
| $V_{GS(th)}$ | Gate Threshold Voltage | 0.4 | 0.67 | 1.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | | | 1 | μA | $V_{DS}$=12V, $V_{GS}$=0V |
| $I_{GSS}$ | Gate-to-Source Leakage Current | | | ±100 | nA | $V_{GS}$=±12V, $V_{DS}$=0V |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55℃ to 150℃ Max | | | | |

## 4. Die Outline




Die Size: 670μm × 590μm (including scribe line)

Gate: 120μm × 120μm

For SOT23-6 package

Suggest Bonding wire:

Gate: 1 × 1.2 mil Cu *2

Source: 4 × 1.2 mil Cu *2