



WANSEMI
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WP2N7002

Enhancement Mode N-Channel Power MOSFET

SOT23/NMOS/60V/±20V/1.6V/0.5A/1.9Ω

Rev1.2



60V, 1.9Ω, 0.5A, N-Channel MOSFET

1. Features

- ◆ Low R_{DS(on)} @VGS =10V
- ◆ 5V Logic Level Control
- ◆ N Channel SOT23 Package
- ◆ HBM ESD Protection 2KV
- ◆ Pb-Free, RoHS Compliant

V _{DS}	R _{DS(on)} Typ.	I _D
60V	1.9Ω @ 10V	0.5A
	1.92Ω @ 4.5V	

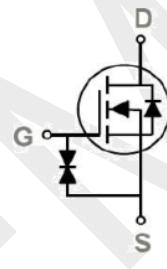
2. Applications

- ◆ LED Lighting Application
- ◆ ON/OFF switch
- ◆ Networking



SOT23

Pin Description



Schematic Diagram

3. Package Marking and Ordering Information

Part no.	Marking	Package	PCS/Reel	PCS/CTN.
WP2N7002	7002	SOT23	3,000	180,000

4. Absolute Max Ratings at Ta=25°C (Note1)

Parameter	Symbol	Maximum	Units
Drain to Source Voltage	V _{DSS}	60	V
Gate to Source Voltage	V _{GSS}	±20	V
Drain Current (DC)	I _D	0.5	A
Drain Current (Pulse), PW≤300μs	I _{DP}	1.8	A
Total Dissipation	P _D	0.3	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-50 to +150	°C

Note 1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



5.Thermal Resistance Ratings (Note 2)

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	400	°C/W

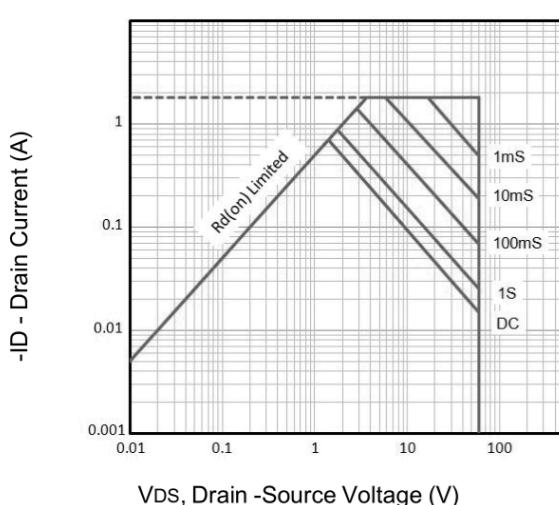
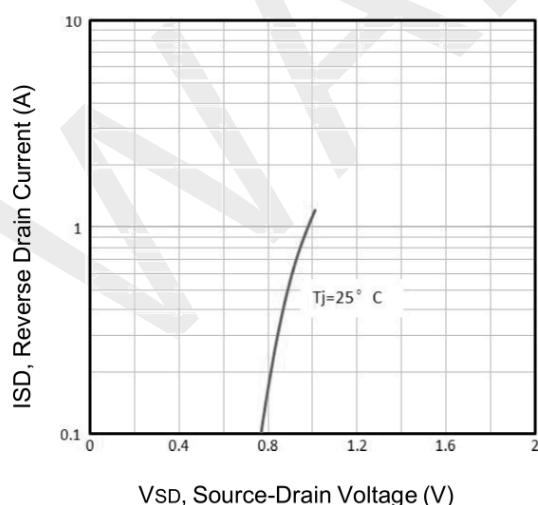
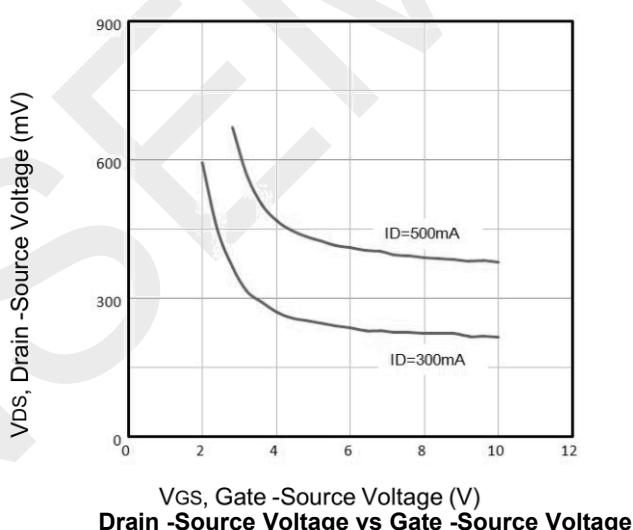
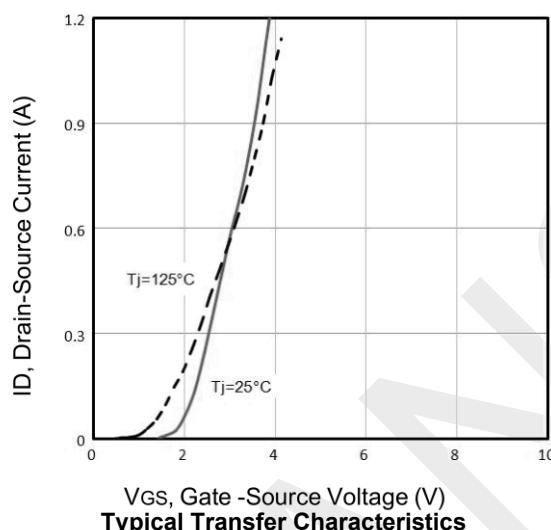
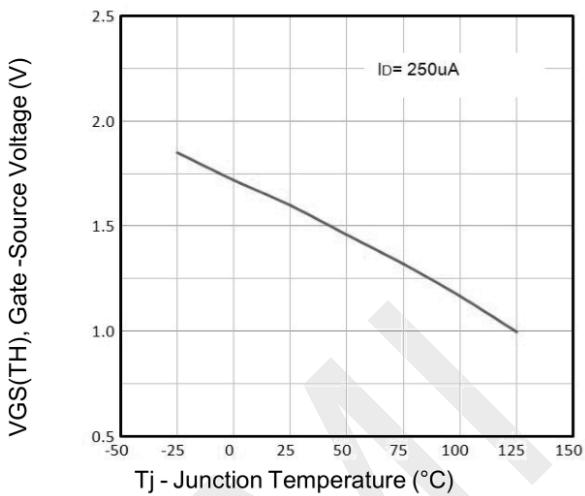
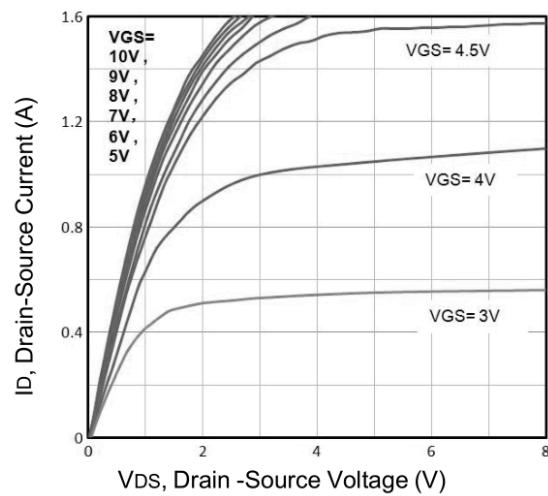
Note 2: When mounted on 1 inch square copper board $t \leq 10\text{sec}$ The value in any given application depends on the user's specific board design.

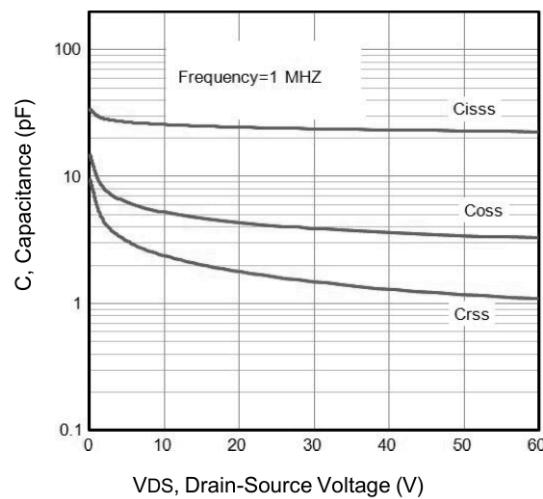
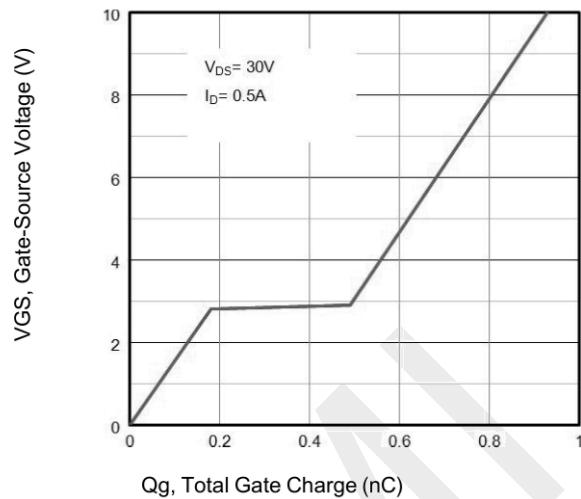
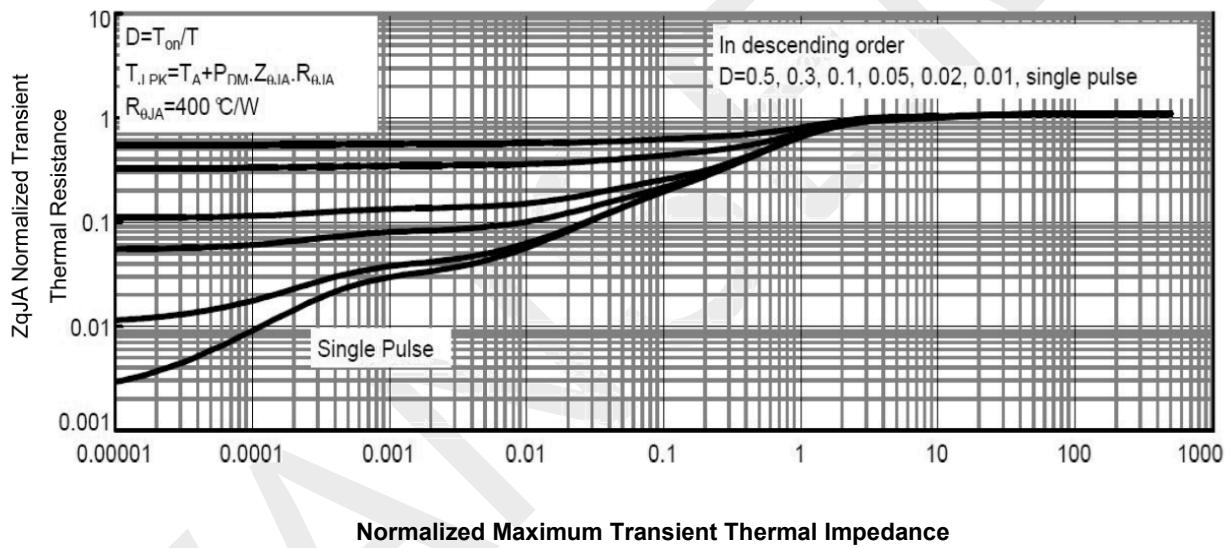
6.Electrical Characteristics at $T_a=25^\circ\text{C}$ (Note 3)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1	uA
Gate to Source Leakage Current	I_{GS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	uA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	1.0	1.6	2.5	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	$I_D = 0.5\text{A}, V_{GS} = 10\text{V}$	-	1.9	2.5	Ω
		$I_D = 0.3\text{A}, V_{GS} = 4.5\text{V}$	-	1.92	3.2	Ω
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}, V_{DS}=30\text{V},$ Frequency=1.0MHz	-	23.8	-	pF
Output Capacitance	C_{oss}		-	3.9	-	pF
Reverse Transfer Capacitance	C_{rss}		-	1.5	-	pF
Turn-ON Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{V}, I_D = 0.3\text{A},$ $R_G = 3.3\Omega, V_{GS} = 10\text{V}$	-	6	-	ns
Rise Time	t_r		-	3.5	-	ns
Turn-OFF Delay Time	$t_{d(off)}$		-	20	-	ns
Fall Time	t_f		-	5.9	-	ns
Total Gate Charge	Q_g	$V_{DS} = 30\text{V},$ $V_{GS} = 10\text{V},$ $I_D = 0.5\text{A}$	-	0.93	-	nC
	Q_{gs}		-	0.18	-	nC
	Q_{gd}		-	0.31	-	nC
Diode Forward Voltage	V_{FSD}	$I_{SD} = 0.5\text{A}, V_{GS} = 0$	-	0.78	1.2	V

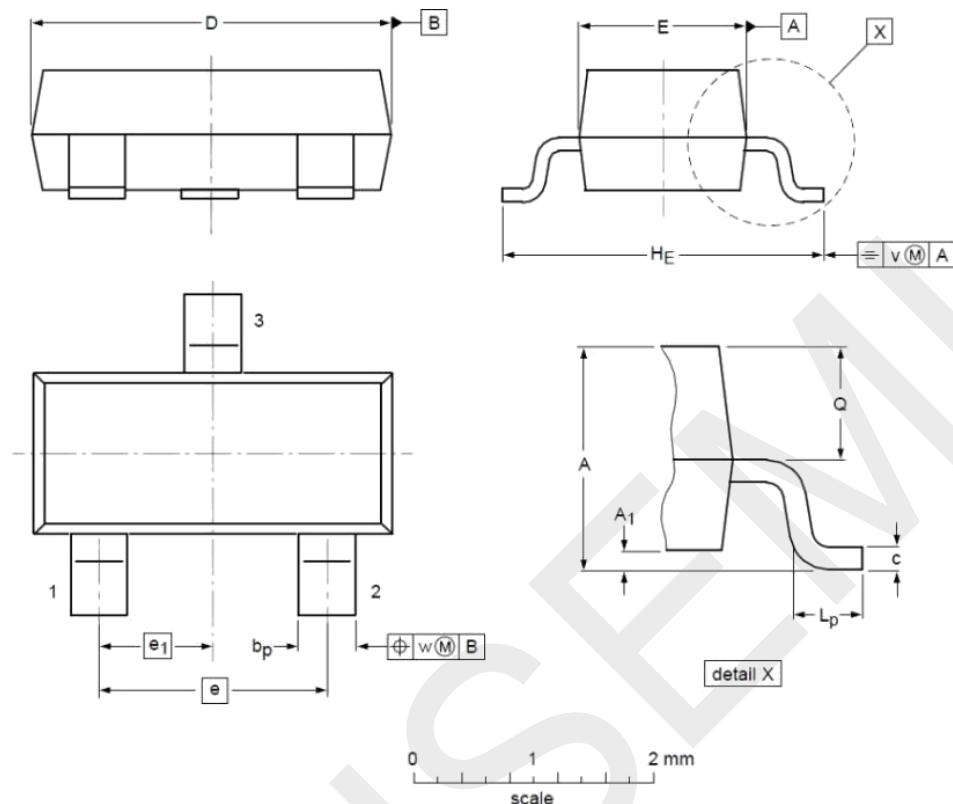
Note 2: Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7.Typical Electrical and Thermal Characteristics




Typical Capacitance Vs. Drain-Source Voltage

Typical Gate Charge Vs. Gate-Source Voltage

Normalized Maximum Transient Thermal Impedance

8.Package Dimensions



DIMENSIONS (unit : mm)

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.90	1.01	1.15	A ₁	0.01	0.05	0.10
b _p	0.30	0.42	0.50	c	0.08	0.13	0.15
D	2.80	2.92	3.00	E	1.20	1.33	1.40
e	--	1.90	--	e ₁	--	0.95	--
H _E	2.25	2.40	2.55	L _p	0.30	0.42	0.50
Q	0.45	0.49	0.55	v	--	0.20	--
w	--	0.10	--				

9.Important Notice

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