# Y0006

# P-Channel Enhancement Mode MOSFET

**-40V(VDS) / ±20V(VGS) / -40A(ID)**

**Rev1.0**

# Wafer Specification

## 1. Order Information

| Part No. | Description | Gross die / per 8" wafer |
|---|---|---|
| Y0006 | **-40V($V_{DS}$) / ±20V($V_{GS}$) / -40A($I_D$)**<br>**P-Channel Enhancement Mode MOSFET** | 6,756 |

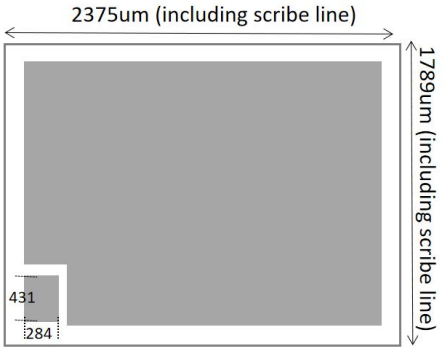
## 2. Mechanical Data

| | |
|---|---|
| Nominal Back Metal Composition, Thickness | Ti-Ni-Ag (13kA°) |
| Nominal Front Metal Composition, Thickness | AlCu (4μm) |
| Wafer Diameter | 200mm, with 010 notch |
| Wafer Thickness | 150μm±10μm |
| Scribe Line Width | 60μm |
| Passivation | SRO+SiN |

## 3. Key Electrical Characteristics of Die（at Tj = 25 °C, unless otherwise specified)

| Parameter | Description | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | -40 | | | V | $V_{GS}$=0V, $I_D$=-250μA |
| $I_{D(Device\ Ref)}$ | Continuous Drain Current | | | -40 | A | $T_J$=25℃ |
| $R_{DS(on)}$(CP) | Static Drain-to-Source On-Resistance | | 7.5 | 15 | mΩ | $V_{GS}$=-10V, $I_D$=-1A |
| | | | 9.5 | 22 | mΩ | $V_{GS}$=-4.5V, $I_D$=-1A |
| $R_{DS(on)}$(FT) | Static Drain-to-Source On-Resistance | | 8 | 13 | mΩ | $V_{GS}$=-10V, $I_D$=-20A |
| | | | 10 | 22 | mΩ | $V_{GS}$=-4.5V, $I_D$=-10A |
| $V_{GS(th)}$ | Gate Threshold Voltage | -1.3 | -1.6 | -2.3 | V | $V_{DS}$=$V_{GS}$, $I_D$=-250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | | | -1 | μA | $V_{DS}$=-40V, $V_{GS}$=0V |
| $I_{GSS}$ | Gate-to-Source Leakage Current | | | ±100 | nA | $V_{GS}$=±20V, $V_{DS}$=0V |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55℃ to 150℃ Max | | | | |

## 4. Die Outline




Die Size: 2375μm × 1789μm (including scribe line)

Gate: 431μm × 284μm

For TO-252 package

Suggest Bonding wire:

Gate: 1 × 1.7 mil Cu

Source: 2× 15 mil AL