

Y0014

P-Channel Enhancement Mode MOSFET

-20V(VDS) / ± 12 V(VGS) / -20A(ID)

Rev1.5



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
Y0014	-20V(V_{DS}) / $\pm 12V(V_{GS})$ / -20A(I_D) P-Channel Enhancement Mode MOSFET	23,798

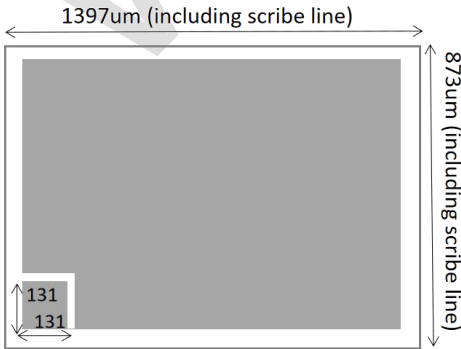
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag(13kÅ°)
Nominal Front Metal Composition, Thickness	AlCu (4µm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	125µm±10µm
Scribe Line Width	60µm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20			V	$V_{GS}=0V$, $I_D=-250\mu A$
$I_{D(\text{Device Ref})}$	Continuous Drain Current			-20	A	$T_J=25^\circ\text{C}$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		10.5	15.5	mΩ	$V_{GS}=-4.5V$, $I_D=-1A$
			14.5	20.5	mΩ	$V_{GS}=-2.5V$, $I_D=-1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		11	16	mΩ	$V_{GS}=-4.5V$, $I_D=-10A$
			15	21	mΩ	$V_{GS}=-2.5V$, $I_D=-5A$
$V_{GS(th)}$	Gate Threshold Voltage	-0.5	-0.8	-1.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			-1	µA	$V_{DS}=-20V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 12V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 1397µm × 873µm (including scribe line)
	Gate: 131µm × 131µm
	For TO-252 package Suggest Bonding wire: Gate: 1 × 1.0 mil Cu Source: 2 × 12 mil AL