

Y0027

P-Channel Enhancement Mode MOSFET

-18V(VDS) / ± 12 V(VGS) / -7A(ID))

Rev0.1



Wafer Specification

1. Order Information

Part No.	Description	Gross die / per 8" wafer
Y0027	-18V(V_{DS}) / ± 12 V(V_{GS}) / -7A(I_D) P-Channel Enhancement Mode MOSFET	29,876

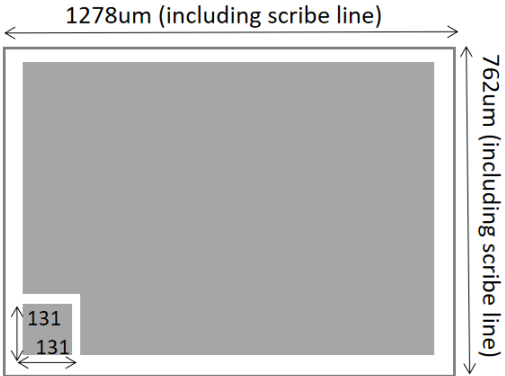
2. Mechanical Data

Nominal Back Metal Composition, Thickness	Ti-Ni-Ag((1kÅ-2kÅ-10kÅ))
Nominal Front Metal Composition, Thickness	AlCu (4μm)
Wafer Diameter	200mm, with 010 notch
Wafer Thickness	125μm±10μm
Scribe Line Width	60μm
Passivation	SRO+SiN

3. Key Electrical Characteristics of Die (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Description	Min.	Typ.	Max.	Unit	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-18			V	$V_{GS}=0V$, $I_D=-250\mu A$
$I_{D(Devic\ Ref)}$	Continuous Drain Current			-7	A	$T_J=25^\circ\text{C}$
$R_{DS(on)}(CP)$	Static Drain-to-Source On-Resistance		11.2	14.3	mΩ	$V_{GS}=-4.5V$, $I_D=-1A$
			14.9	18.9	mΩ	$V_{GS}=-2.5V$, $I_D=-1A$
$R_{DS(on)}(FT)$	Static Drain-to-Source On-Resistance		12.2	15.3	mΩ	$V_{GS}=-4.5V$, $I_D=-7A$
			15.9	19.9	mΩ	$V_{GS}=-2.5V$, $I_D=-5A$
$V_{GS(th)}$	Gate Threshold Voltage	-0.3	-0.7	-1.5	V	$V_{DS}=V_{GS}$, $I_D=-250\mu A$
I_{DSS}	Drain-to-Source Leakage Current			-1	μA	$V_{DS}=-12V$, $V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current			±100	nA	$V_{GS}=\pm 12V$, $V_{DS}=0V$
T_J , T_{STG}	Operating and Storage Temperature	-55°C to 150°C Max				

4. Die Outline

	Die Size: 1278μm × 762μm (including scribe line)
	Gate: 131μm × 131μm
	For SOT23-3L package Suggest Bonding wire: Gate: 1*42μm Cu Source: 10*42μm Cu 