WANSEMI
万代半导体

WP4606K

Enhancement Mode N+P-Channel Power MOSFET

SOP8/N+PMOS/30V/±20V/1.7V/5.5A/14.5mΩ

-30V/±20V/-1.7V/-4.2A/33mΩ

Rev0.8

30V N+P-Channel MOSFET

1.Features

- High power and current handing capability
- Lead free product is acquired
- Fast switching
- Surface mount package

- N-Channel

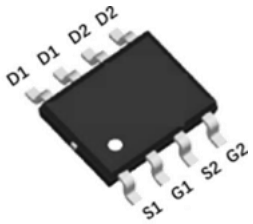
V_{DS}	$R_{DS(on)}$ Typ.	I_D
30V	14.5mΩ @ 10V	5.5A
	23.5mΩ @ 4.5V	

- P-Channel

V_{DS}	$R_{DS(on)}$ Typ.	I_D
-30V	33mΩ @ -10V	-4.2A
	45mΩ @ -4.5V	

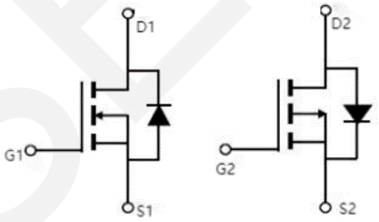
2.Applications

- Power Switching Application
- Load Switching
- BLDC Motor driver



SOP8

Pin Description



N-Channel P-Channel

Schematic Diagram

3.Package Marking and Ordering Information

Part no.	Marking	Package	PCS/Reel	PCS/CTN.
WP4606K	•4606	SOP8	4,000	48,000

4.Absolute Max Ratings at Ta=25℃ (Note1)

Parameter		Symbol	N-chanel	P-chanel	Units
Drain to Source Voltage		V_{DSS}	30	-30	V
Gate to Source Voltage		V_{GSS}	±20	±20	V
Drain Current (DC),	TA=25 °C	I_D	5.5	-4.2	A
Drain Current (Pulse), PW≤300μs		I_{DM}	22	-16.8	A
Avalanche Energy, Single Pulsed		E_{AS}	30	25	mJ
Total Dissipation	TA=25 °C	P_D	2.0	2.0	W
Junction Temperature		T_j	150	150	℃

Parameter	Symbol	N-chanel	P-chanel	Units
Storage Temperature	T_{stg}	-55 to +150	-55 to +150	℃

Note 1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5.Thermal Resistance Ratings (Note 2)

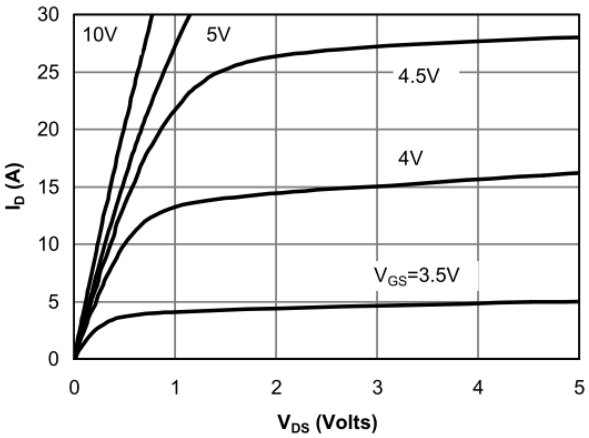
Parameter	Symbol	Value	Unit
Maximum Junction-to-Ambient	$R_{\theta JA}$	62.5	℃/W

Note 2：When mounted on 1 inch square copper board t ≤ 10sec The value in any given application depends on the user's specific board design.

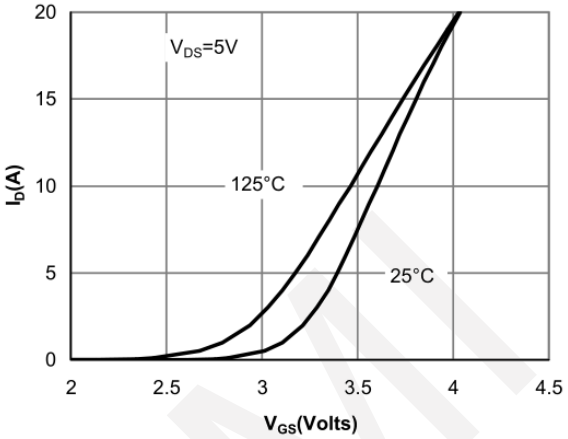
6.NMOS Electrical Characteristics at Ta=25℃ (Note 3)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250μA, V_{GS} = 0V	30	-	-	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	-	-	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_{DS}=250μA	1.0	1.7	2.5	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	I_D = 5.5A, V_{GS} = 10V	-	14.5	23	mΩ
		I_D = 5.5A, V_{GS} = 4.5V	-	23.5	35	mΩ
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, Frequency=1.0MHz	-	457	-	pF
Output Capacitance	C_{oss}		-	74	-	pF
Reverse Transfer Capacitance	C_{rss}		-	63	-	pF
Turn-ON Delay Time	$t_{d(on)}$	V_{DD} = 15V, V_{GS} = 10V, R_{GEN} = 3Ω, I_D = 3A	-	10	-	ns
Rise Time	t_r		-	15	-	ns
Turn-OFF Delay Time	$t_{d(off)}$		-	30	-	ns
Fall Time	t_f		-	6	-	ns
Total Gate Charge	Q_g	V_{DS} = 15V, V_{GS} = 10V, I_D = 5.5A	-	10	-	nC
	Q_{gs}		-	1	-	nC
	Q_{gd}		-	2.3	-	nC
Diode Forward Voltage	V_{FSD}	I_S = 5.5A, V_{GS} = 0V	-	0.85	1.2	V

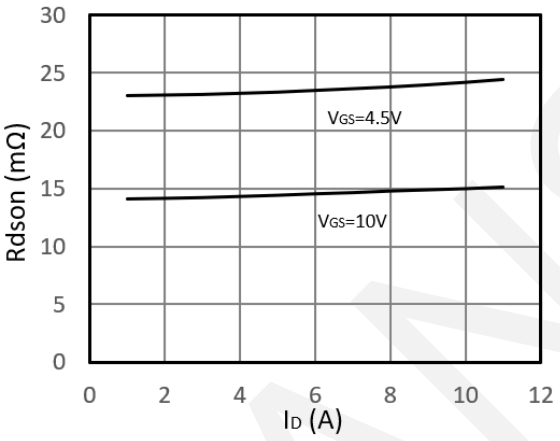
NMOS Typical electrical and thermal characteristics



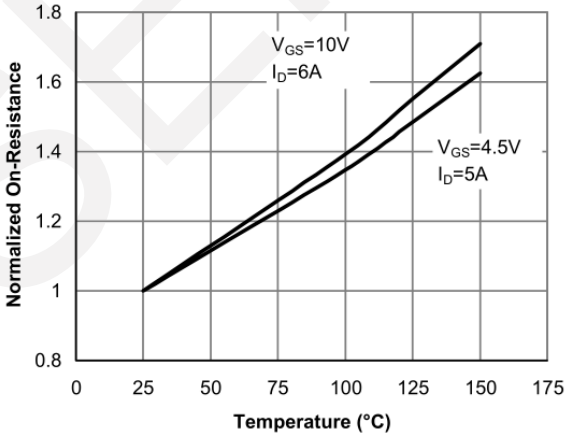
Output Characteristics



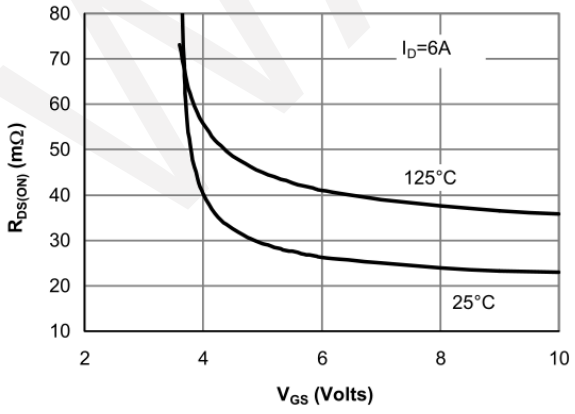
Transfer Characteristics



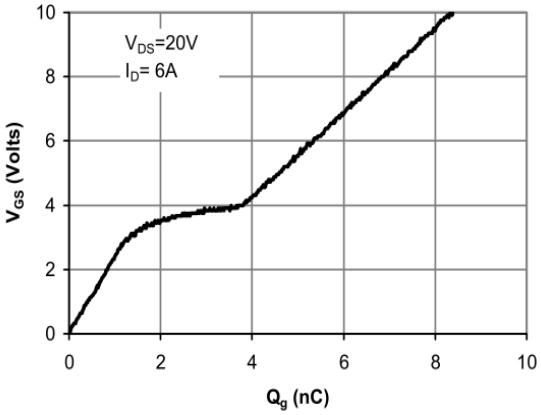
Drain-Source On-Resistance



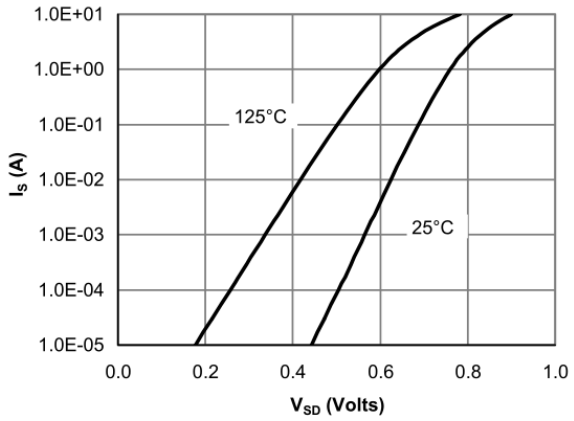
Drain-Source On-Resistance



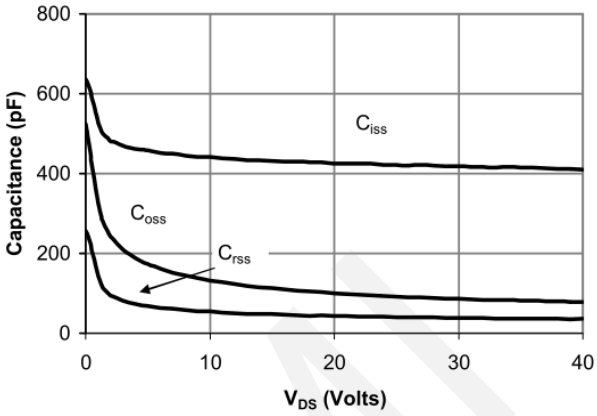
Rdson vs Vgs



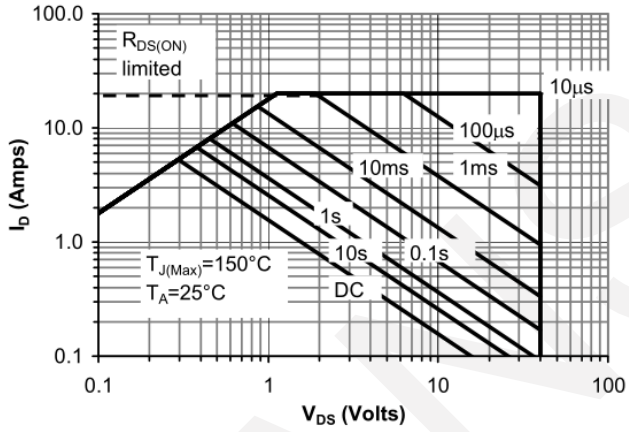
Gate Charge



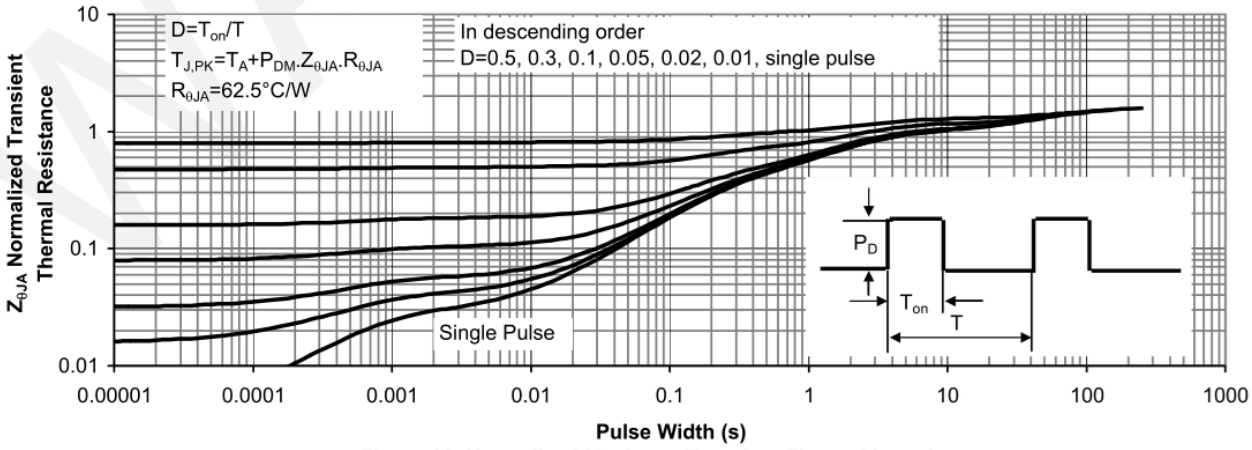
Source- Drain Diode Forward



Capacitance vs Vds



Safe Operating Area



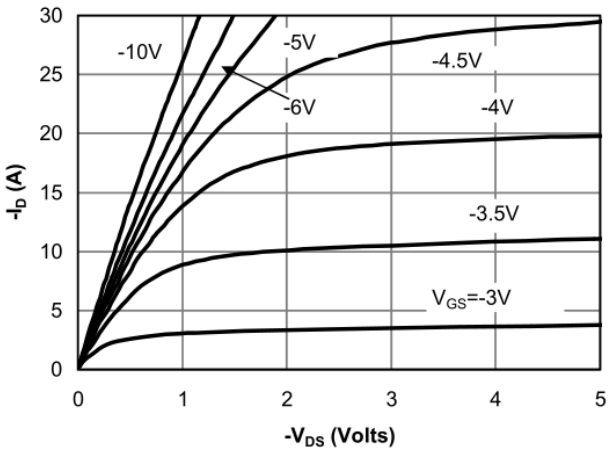
Normalized Maximum Transient Thermal Impedance

7.PMOS Electrical Characteristics at Ta=25℃

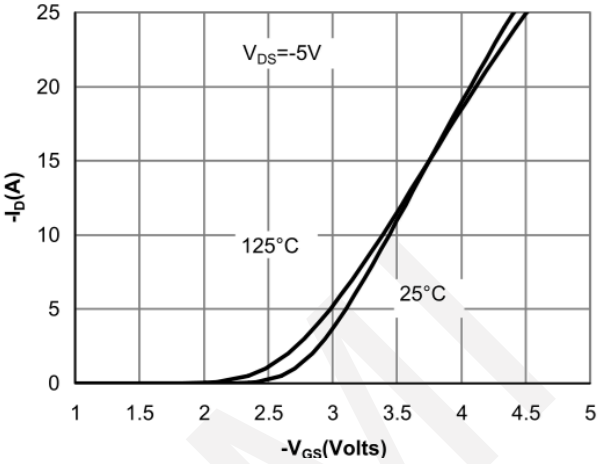
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -250μA, V_{GS} = 0V	-30	-	-	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	-	-	-1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_{DS}=-250μA	-1.0	-1.7	-2.5	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	I_D = -4.2A, V_{GS} =-10V	-	33	40	mΩ
		I_D =-4.2A, V_{GS} =-4.5V	-	45	65	mΩ
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, Frequency=1.0MHz	-	550	-	pF
Output Capacitance	C_{oss}		-	85	-	pF
Reverse Transfer Capacitance	C_{rss}		-	75	-	pF
Turn-ON Delay Time	$t_{d(on)}$	V_{DD} = -15V, V_{GS} = -10V, R_{GEN} =3Ω, I_D = -3A	-	9.5	-	ns
Rise Time	t_r		-	5.5	-	ns
Turn-OFF Delay Time	$t_{d(off)}$		-	42.5	-	ns
Fall Time	t_f		-	13.6	-	ns
Total Gate Charge	Q_g	V_{DS} = -15V, V_{GS} = -10V, I_D = -1A	-	11	-	nC
	Q_{gs}		-	2.5	-	nC
	Q_{gd}		-	3	-	nC
Diode Forward Voltage	V_{FSD}	I_S = -4.2A, V_{GS} = 0V	-	-	-1.2	V

Note 3：Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different condit

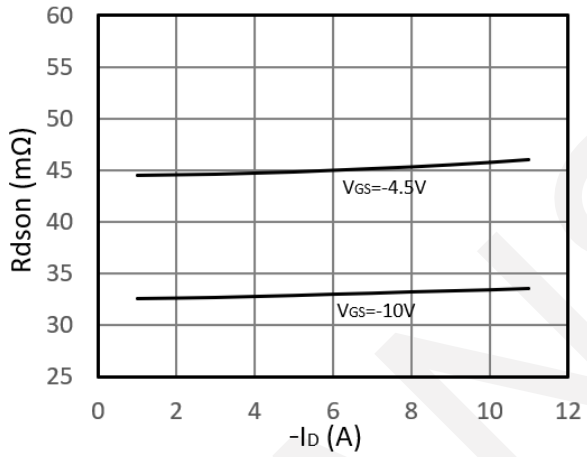
PMOS Typical electrical and thermal characteristics



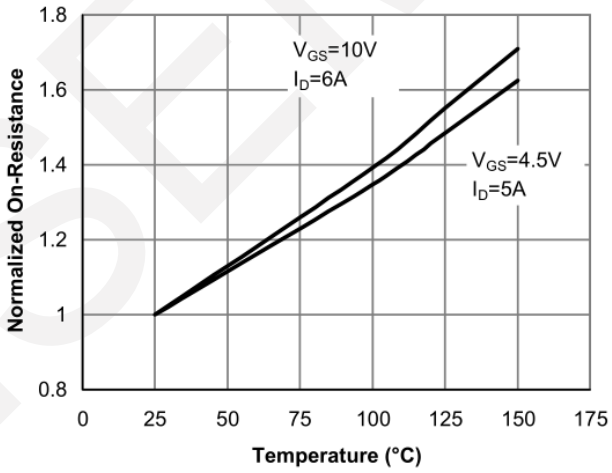
Output Characteristics



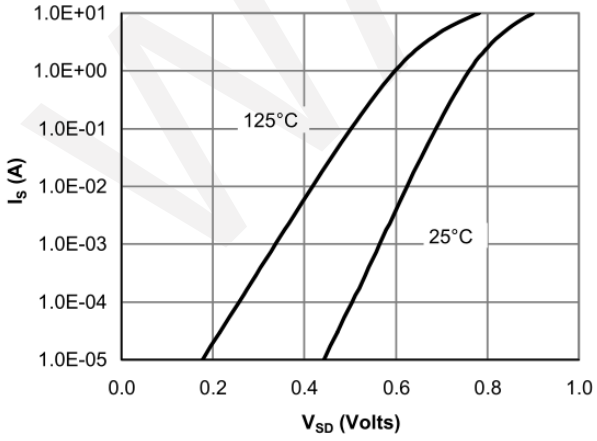
Transfer Characteristics



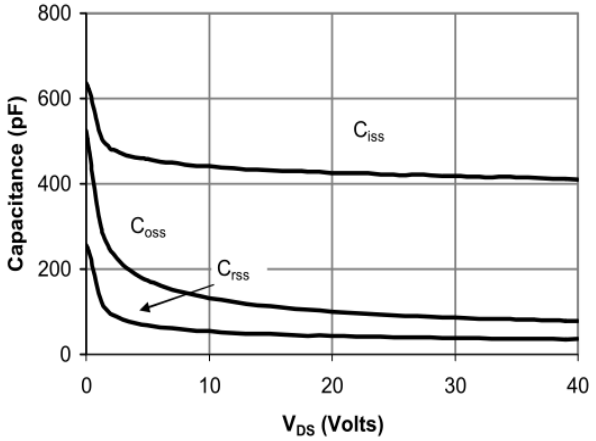
Rdson- Drain Current



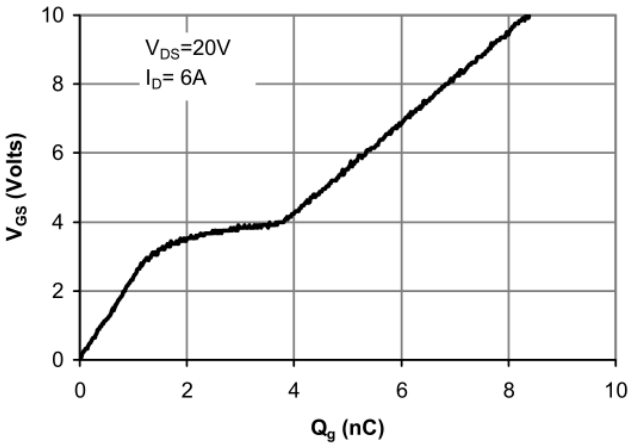
Rdson-Junction Temperature



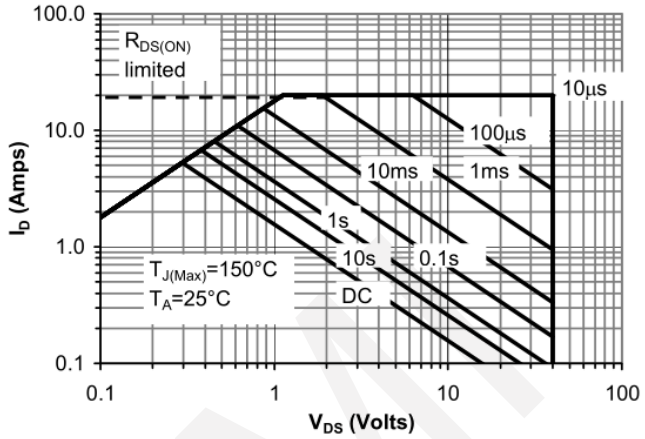
Source- Drain Diode Forward



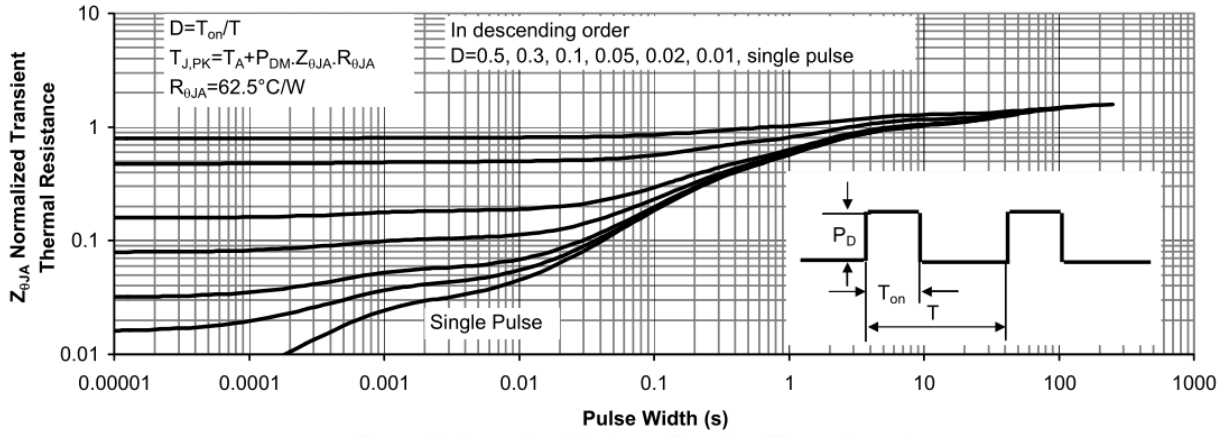
Capacitance vs Vds



Gate-Charge

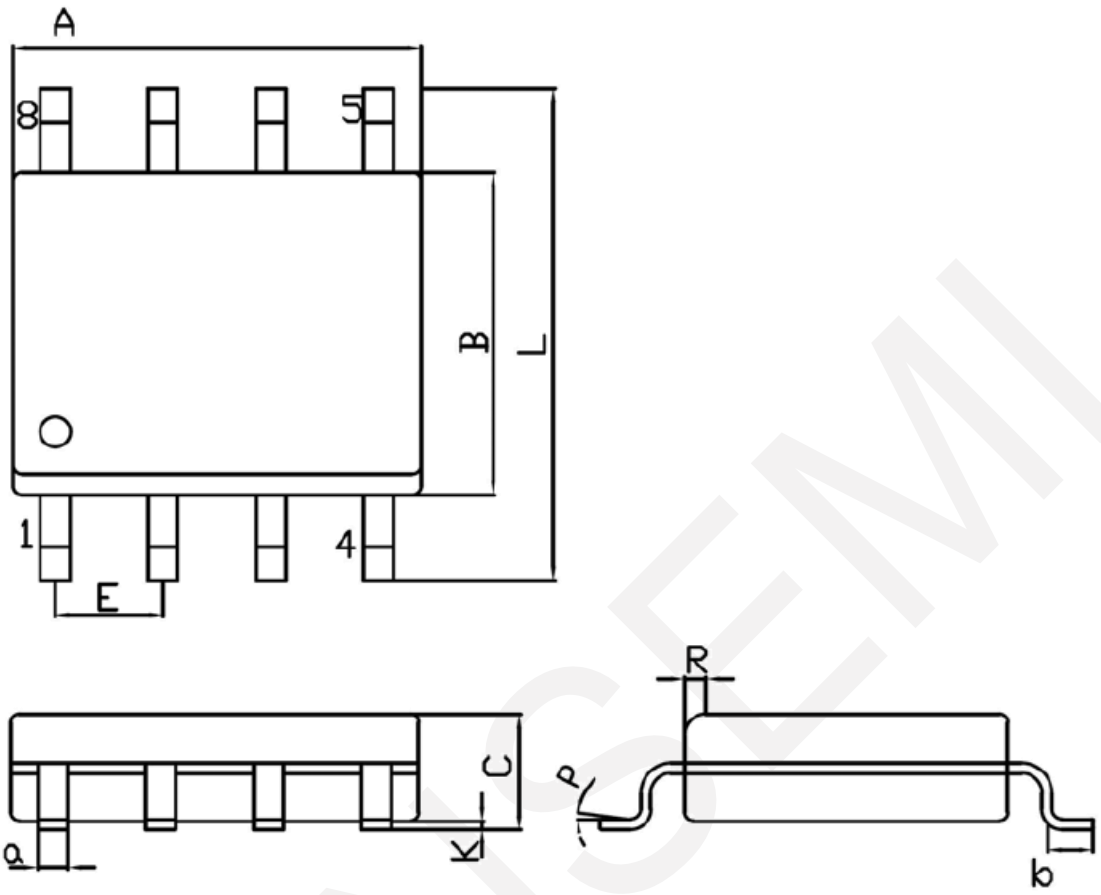


Safe Operation Area



Normalized Maximum Transient Thermal Impedance

8.Package Dimensions



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.35	1.75
B	3.70	4.10	a	0.35	0.49
L	5.80	6.20	R	0.30	0.60
E	1.27BSC		P	0°	7°
K	0.12	0.22	b	0.40	1.25

9. Important Notice

WAN SEMICONDUCTOR (NINGBO) CO.,LTD reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services and to discontinue any product or service. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to WANSEMI’s terms and conditions of sale supplied at the time of order acknowledgment.

WANSEMI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in WANSEMI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent WANSEMI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

WANSEMI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using WANSEMI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

No WANSEMI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Unless WANSEMI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use, WANSEMI will not be responsible for any failure of such components to meet such requirements.